What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate having a main surface along which a semiconductor element is formed;

interlayer insulating films formed on said main surface;

conductive interconnections provided in a plurality of layers separated by said interlayer insulating films;

conductive dummy interconnections provided in the same layers as said interconnections in two or more layers included in said plurality of layers; and

a conductive dummy plug selectively buried in said interlayer insulating films to connect said dummy interconnections between said two or more layers and connected together with said dummy interconnections to a stable potential line which is included in said interconnections and which holds a constant potential with respect to a potential carried on a lower-potential power-supply line or a higher-potential power-supply line.

2. A semiconductor device comprising:

a semiconductor substrate having a main surface in which an element isolation structure for isolating said main surface into a plurality of regions is selectively formed, each of said plurality of regions having a semiconductor element formed therein;

interlayer insulating films formed on said main surface;

conductive interconnections provided in a plurality of layers separated by said interlayer insulating films;

conductive dummy interconnections provided in the same layers as said interconnections in two or more layers included in said plurality of layers;

a conductive dummy plug selectively buried in said interlayer insulating films to connect said dummy interconnections between said two or more layers;

a conductive layer formed in a part of said element isolation structure; and

another conductive plug selectively buried in said interlayer insulating films to connect said conductive layer and said dummy interconnections.

3. The semiconductor device according to claim 2, wherein said dummy interconnections and said dummy plug are connected to a stable potential line which is included in said interconnections and which holds a constant potential with respect to a potential carried on a lower-potential power-supply line or a higher-potential power-supply line.

4. The semiconductor device according to claim 3, wherein said plurality of regions correspond to a plurality of functional blocks in an integrated circuit, and

each of said plurality of functional blocks is surrounded by said conductive layer together with said element isolation structure.

5. The semiconductor device according to claim 2, wherein a trench is formed in part of said element isolation structure and said conductive layer is buried in said trench.

6. The semiconductor device according to claim 2, wherein said semiconductor substrate further comprises a buried insulating layer,

said element isolation structure comprises a part connected to said buried insulating layer, and

said conductive layer selectively extends through said part of said element isolation structure to reach said buried insulating layer.

7. The semiconductor device according to claim 1, wherein said dummy interconnections are provided to sandwich an interconnection part included in said interconnections in at least one of said two or more layers.

8. The semiconductor device according to claim 7, wherein said dummy interconnections also comprise a dummy interconnection which is provided in a layer located over said at least one layer to cover said interconnection part.

9. The semiconductor device according to claim 1, wherein said stable potential line is any of said lower-potential power-supply line, said higher-potential power-supply line, a precharge line included in said interconnections and carrying a precharge potential, and a substrate potential line included in said interconnections and carrying a substrate potential.

10. The semiconductor device according to claim 1, wherein at least one of said dummy interconnections has repetitive protrusions and recesses along its elongate direction in a section taken along said main surface.

11. The semiconductor device according to claim 1, wherein at least one of said dummy interconnections has repetitive protrusions and recesses along its elongate direction in a section taken along a plane perpendicular to said main surface.

12. The semiconductor device according to claim 11, wherein the protrusions among said repetitive protrusions and recesses are connected to a part of said dummy interconnection provided in a lower layer.

13. The semiconductor device according to claim 1, further comprising a passivation film covering the uppermost layer among said plurality of layers and having a higher thermal conductivity than said interlayer insulating films.

14. The semiconductor device according to claim 13, further comprising a heat sink which is in contact with said passivation film.

15. The semiconductor device according to claim 14, wherein said dummy interconnections also comprise one which is provided in said uppermost layer, and

said semiconductor device further comprises another conductive dummy plug selectively buried in said passivation film to connect said heat sink and part of said dummy interconnection which belongs to said uppermost layer.

16. The semiconductor device according to claim 3, wherein said dummy interconnections are provided to sandwich an interconnection part included in said interconnections in at least one of said two or more layers.

17. The semiconductor device according to claim 3, wherein said stable potential line is any of said lower-potential power-supply line, said higher-potential power-supply line, a precharge line included in said interconnections and carrying a precharge potential, and a substrate potential line included in said interconnections and

carrying a substrate potential.

18. The semiconductor device according to claim 2, wherein at least one of said dummy interconnections has repetitive protrusions and recesses along its elongate direction in a section taken along said main surface.

19. The semiconductor device according to claim 2, wherein at least one of said dummy interconnections has repetitive protrusions and recesses along its elongate direction in a section taken along a plane perpendicular to said main surface.

20. The semiconductor device according to claim 2, further comprising a passivation film covering the uppermost layer among said plurality of layers and having a higher thermal conductivity than said interlayer insulating films.